Application Note

AN_INLC_06

January 2019
Revision 1.0

ISELED – EMI Guideline

1. Introduction

This document provides guidance on how to create a PCB layout with ISELED components and build an EMI and EMC robust system design. The contents of this document are to be understood exclusively as guidelines and do not guarantee the fulfilment of certain requirements.

List of Abbreviations and Acronyms

EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
GND	Ground
MCU	Microcontroller Unit
PCB	Printed Circuit Board
STP	Shielded Twisted Pair
UTP	Unshielded Twisted Pair

2. System Design

2.1. System on One PCB

The ISELED communicaton signals are GND-referenced and therefore require a low common mode noise. With a system on a single PCB, the best possible EMI/EMC performance can be achieved.

The communication between the MCU and the first ISELED device is single ended. The capacitive load on these signals significantly determines the maximum distance. Since the capacitive load increases with increasing transmission line length, the distance should be kept as small as possible.

It does not matter which ISELED product is first in line - it can be a smart RGB LED or the INLC100Q16.

The communication of the following components is differential and therefore less susceptible to interference.

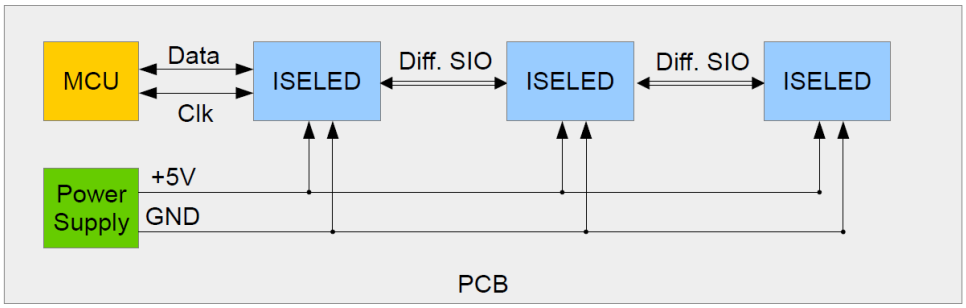


Figure 1 - System of one PCB

2.2. System on Two PCBs

It is also possible to build a system on two PCBs. For the cable connection between the boards two options are possible, which are described in the following. The maximum cable length is limited by the EMI/EMC requirements.

2.2.1. Shielded Twisted Pair (STP)

On the one hand, an STP cable can be used. The cable shield should have a high attenuation and be capacitively coupled to ground. The cable should have two pairs of wires that are twisted and are used for the two SIO signals and the power supply.

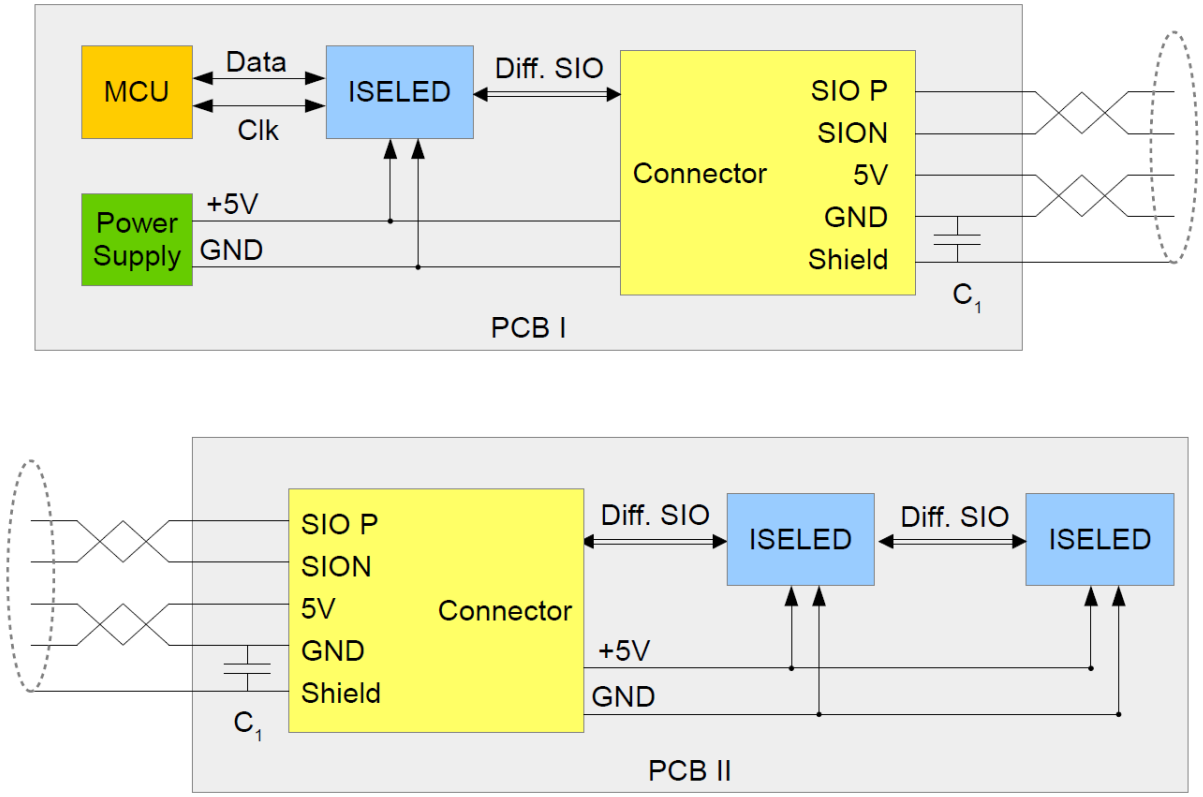


Figure 2 - System on two PCBs with STP cable

2.2.2. Unshielded Twisted Pair (UTP)

Alternatively an unshielded twisted pair cable can be used. In this case, additional filter components should be used between the connector and the last/first ISELED device. The filter should consist of a common mode choke and two ground-coupled capacitors which are connected to the differential signals. The dimensioning of these components is determined by the PCB layout, connector type, cable type, cable length and EMI/EMC requirements.

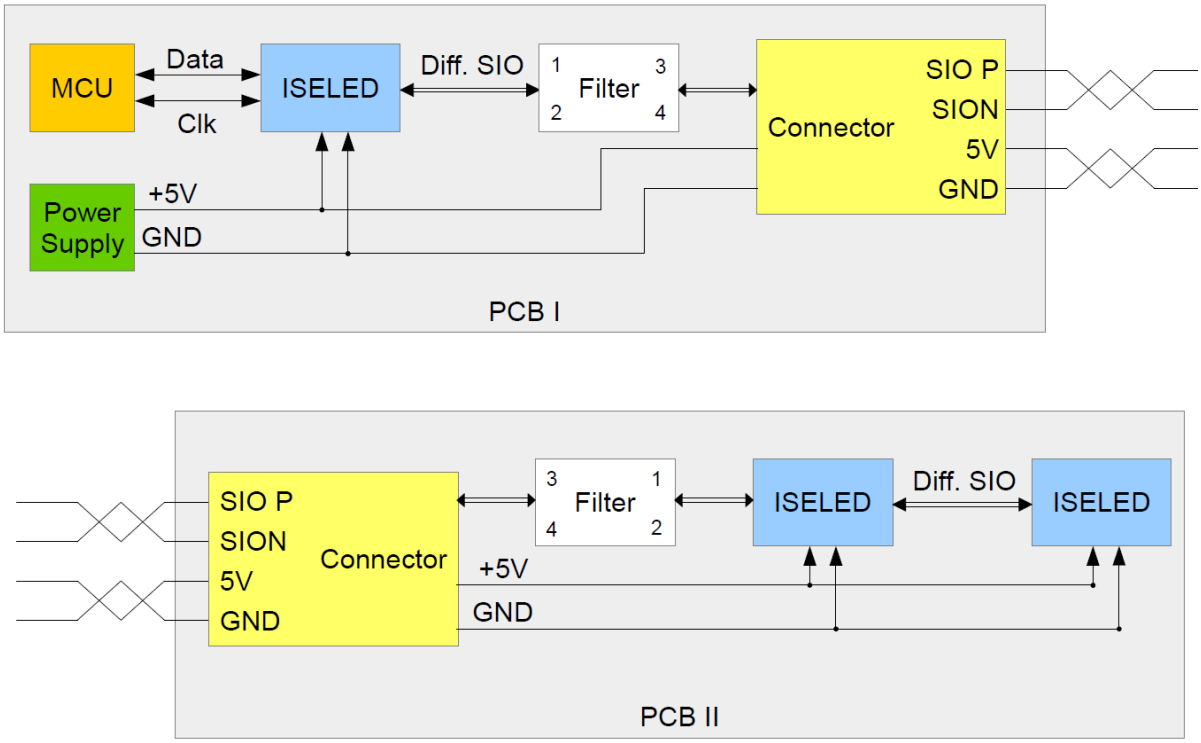


Figure 3 - System on two PCBs with UTP cable

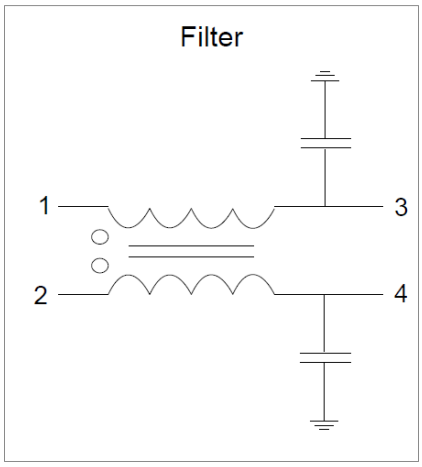


Figure 4 - Filter components

3. PCB Layout

3.1. Capacitor Placement

The smaller capacitor is used in order to support the supply voltage Vcc of the chip and to filter voltage drops that are caused by external events. This ensures that no under-votlage impairs the functionality of the chip. The capacitor should be placed as close as possible to the VCC5 pin where small current peaks flow in a very short time.

The large capacitor is used to support the LED voltage. Here, higher currents occur, which are switched on and off by PWM. Due to the high currents, voltage drops would occur without the capacitor, which would raise and lower the local GND level. This would lead to unwanted emissions. In order to achieve the best possible result, the capacitor should be placed as close as possible to the LEDs or LED supply pin of the smartRGB products.

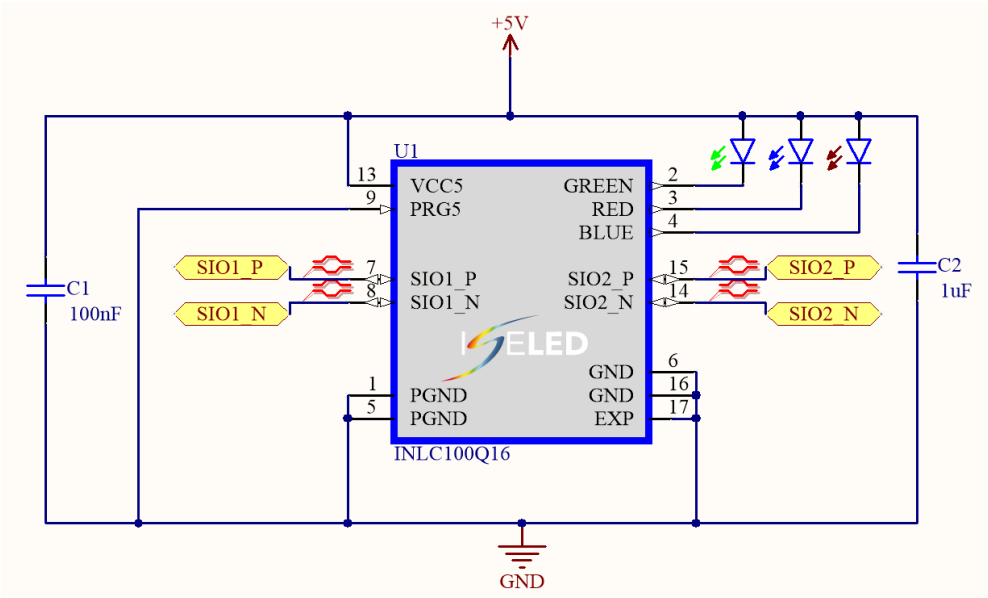


Figure 5 – INLC100Q16 schematic

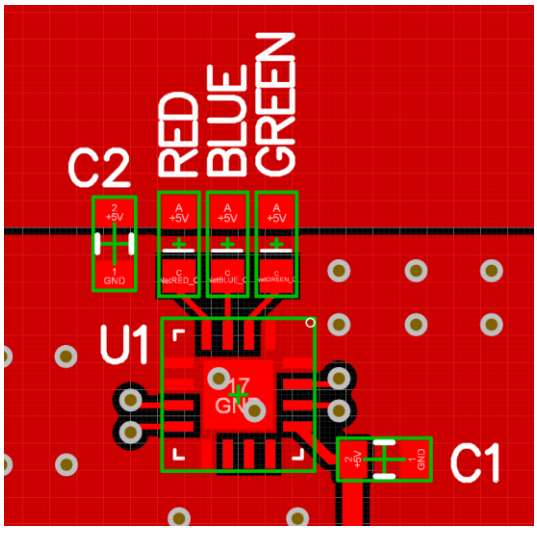


Figure 6 - Capacitor placement

3.2. Differential Routing

3.2.1. Two Layer PCB

For a two layer PCB it is recommended to flood both layers – top and bottom - with GND. The differential traces should be routed on the side opposite the LEDs. The trace impedance Z_0 is 100Ω.

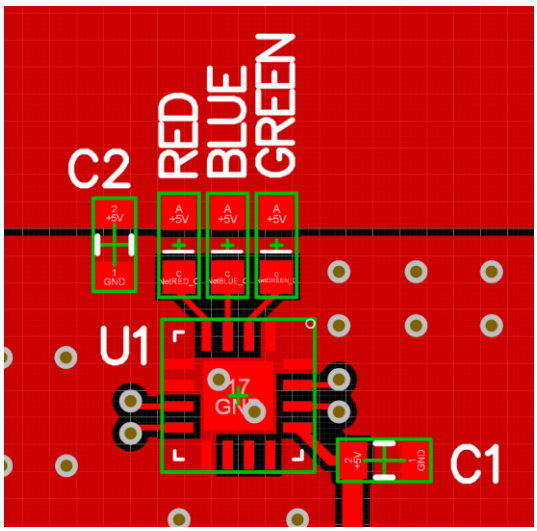
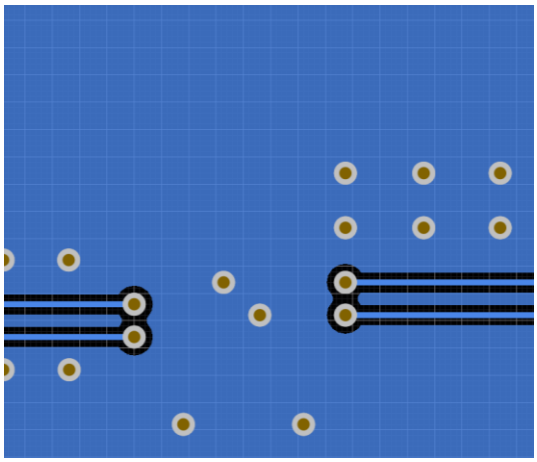
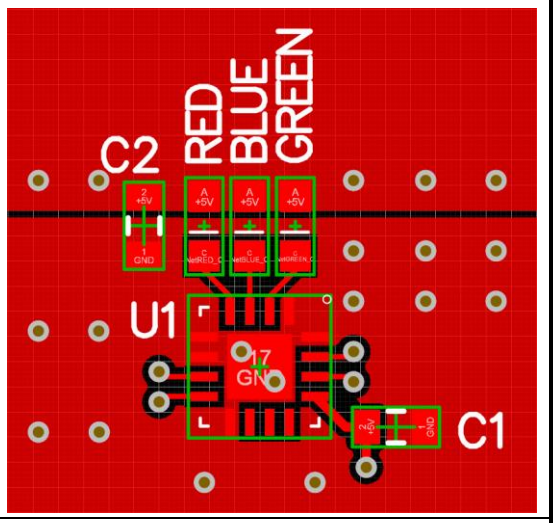
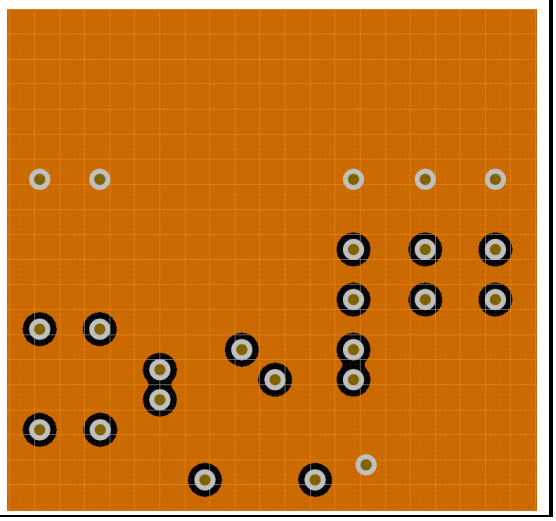
Layer	Plane Net	Example
Top	GND	
Bottom	GND	

Table 1 – Two layer PCB layout example

3.2.2. Four Layer PCB

For optimum shielding of common mode noise, a four layer board is recommended, where the communication traces are routed on the inside layers and are protected by surrounding GND planes.

Layer	Plane Net	Example
Top	GND	
Signal 1	5V	

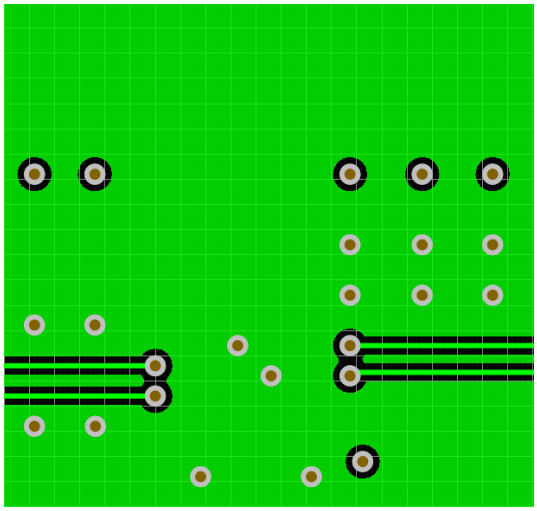
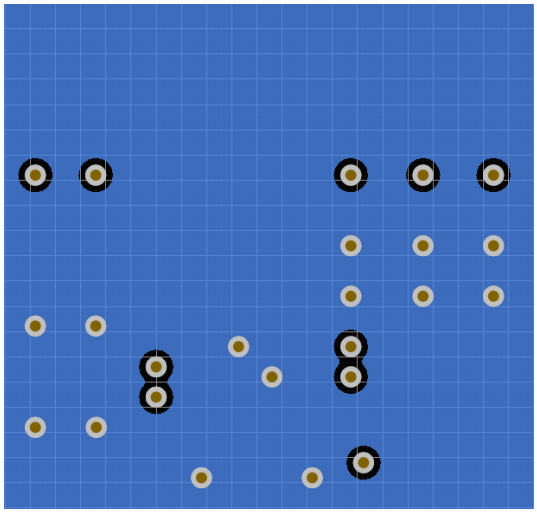
Signal 2	GND	
Bottom	GND	

Table 2 – Four layer PCB layout example

4. Revision History

Revision	Date	Changes
1.0	January 2019	Initial release

Table 3 - Revision history

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